

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040025122 A1	20040205	56	Hardware-based HDL code coverage and design analysis	716/4
2	US 20040019857 A1	20040129	49	Method and apparatus for specifying encoded sub-networks	716/1
3	US 20030217350 A1	20031120	49	Method and apparatus for producing a circuit description of a design	716/18
4	US 20030217340 A1	20031120	48	Method and apparatus for performing technology mapping	716/3
5	US 20030217339 A1	20031120	48	Method and apparatus for performing technology mapping	716/3
6	US 20030182642 A1	20030925	57	Hardware debugging in a hardware description language	716/4
7	US 20030159116 A1	20030821	48	Method and apparatus for specifying encoded sub-networks	716/3
8	US 20030159115 A1	20030821	48	Method and apparatus for performing technology mapping	716/3
9	US 20030154449 A1	20030814	48	Method and apparatus for performing technology mapping	716/3
10	US 20030154448 A1	20030814	48	Method and apparatus for producing a circuit description of a design	716/3
11	US 20030131325 A1	20030710	96	Method and user interface for debugging an electronic system	716/4
12	US 6622291 B1	20030916	31	Method and apparatus for physical budgeting during RTL floorplanning	716/9
13	US 6618839 B1	20030909	55	Method and system for providing an electronic system design with enhanced debugging capabilities	716/4
14	US 6606588 B1	20030812	141	Design apparatus and a method for generating an implementable description of a digital system	703/15
15	US 6581191 B1	20030617	57	Hardware debugging in a hardware description language	716/4

	Document ID	Issue Date	Pages	Title	Current OR
16	US 6543036 B1	20030401	34	Non-linear, gain-based modeling of circuit delay for an electronic design automation system	716/6
17	US 6529861 B1	20030304	24	Power consumption reduction for domino circuits	703/14
18	US 6470482 B1	20021022	42	METHOD AND SYSTEM FOR CREATING, DERIVING AND VALIDATING STRUCTURAL DESCRIPTION OF ELECTRONIC SYSTEM FROM HIGHER LEVEL, BEHAVIOR-ORIENTED DESCRIPTION, INCLUDING INTERACTIVE SCHEMATIC DESIGN AND SIMULATION	716/6
19	US 6467068 B1	20021015	48	Construction of a technology library for use in an electronic design automation system that converts the technology library into non-linear, gain-based models for estimating circuit delay	716/6
20	US 6446240 B1	20020903	46	Evaluation of a technology library for use in an electronic design automation system that converts the technology library into non-linear, gain-based models for estimating circuit delay	716/2
21	US 6425110 B1	20020723	22	Incremental design tuning and decision mediator	716/2
22	US 6421818 B1	20020716	80	Efficient top-down characterization method	716/18
23	US 6421808 B1	20020716	50	Hardware design language for the design of integrated circuits	716/1
24	US 6378123 B1	20020423	81	Method of handling macro components in circuit design synthesis	716/18

	Document ID	Issue Date	Pages	Title	Current OR
25	US 6378116 B1	20020423	13	Using budgeted required time during technology mapping	716/7
26	US 6324678 B1	20011127	45	Method and system for creating and validating low level description of electronic design	716/18
27	US 6295636 B1	20010925	82	RTL analysis for improved logic synthesis	716/18
28	US 6292931 B1	20010918	81	RTL analysis tool	716/18
29	US 6289498 B1	20010911	81	VDHL/Verilog expertise and gate synthesis automation system	716/18
30	US 6289491 B1	20010911	80	Netlist analysis tool by degree of conformity	716/5
31	US 6263483 B1	20010717	81	Method of accessing the generic netlist created by synopsys design compiler	716/18
32	US 6237127 B1	20010522	40	Static timing analysis of digital electronic circuits using non-default constraints known as exceptions	716/6
33	US 6216252 B1	20010410	53	Method and system for creating, validating, and scaling structural description of electronic device	716/1
34	US 6205572 B1	20010320	79	Buffering tree analysis in mapped design	716/5
35	US 6173435 B1	20010109	80	Internal clock handling in synthesis script	716/18
36	US 6080201 A	20000627	15	Integrated placement and synthesis for timing closure of microprocessors	703/14
37	US 5933356 A	19990803	43	Method and system for creating and verifying structural logic model of electronic design from behavioral description, including generation of logic and timing models	703/15

	Document ID	Issue Date	Pages	Title	Current OR
38	US 5910897 A	19990608	32	Specification and design of complex digital systems	716/19
39	US 5880971 A	19990309	26	Methodology for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from semantic specifications and descriptions thereof	716/6
40	US 5870308 A	19990209	49	Method and system for creating and validating low-level description of electronic design	716/18
41	US 5867399 A	19990202	64	System and method for creating and validating structural description of electronic system from higher-level and behavior-oriented description	716/18
42	US 5801958 A	19980901	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/18
43	US 5623418 A	19970422	66	System and method for creating and validating structural description of electronic system	716/1
44	US 5598344 A	19970128	51	Method and system for creating, validating, and scaling structural description of electronic device	716/18
45	US 5572437 A	19961105	44	Method and system for creating and verifying structural logic model of electronic design from behavioral description, including generation of logic and timing models	716/18

	Document ID	Issue Date	Pages	Title	Current OR
46	US 5572436 A	19961105	48	Method and system for creating and validating low level description of electronic design	716/18
47	US 5557531 A	19960917	47	Method and system for creating and validating low level structural description of electronic design from higher level, behavior-oriented description, including estimating power dissipation of physical implementation	716/1
48	US 5555201 A	19960910	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/1
49	US 5553002 A	19960903	47	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, using milestone matrix incorporated into user-interface	716/11
50	US 5544067 A	19960806	43	Method and system for creating, deriving and validating structural description of electronic system from higher level, behavior-oriented description, including interactive schematic design and simulation	703/14

	Document ID	Issue Date	Pages	Title	Current OR
51	US 5544066 A	19960806	47	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of low-level design constraints	716/18
52	US 5541849 A	19960730	46	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters	716/18
53	US 5526277 A	19960611	31	ECAD system for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from high-level semantic descriptions thereof	716/3
54	US 5493508 A	19960220	31	Specification and design of complex digital systems	716/5
55	US 5452239 A	19950919	131	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementation of the netlist in a hardware emulation system	703/19
56	US 5222030 A	19930622	528	Methodology for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from high-level semantic specifications and descriptions thereof	716/11